WE CLAIM:

1. A process of fabricating conductive structures in features of an insulator layer on a substrate comprising:

applying a layer of conductive material over the insulator layer so that the layer of conductive material covers field regions adjacent said features and fills in said features,

establishing a grain size differential between the conductive material which covers said field regions and the conductive material which fills in said features by annealing said layer of conductive material, and

removing excess conductive material to uncover said field regions and leave said conductive structures.

2. The process according to claim 1, wherein said layer of conductive material is applied so as to define a first layer thickness over said field regions and a second layer thickness in and over said features.

3. The process according to claim 2, wherein said first layer thickness and said second layer thickness are dimensioned such that $d_1 \leq 0.5d_2$, with d_1 being said first layer thickness and d_2 being said second layer thickness.

4. The process according to claim 3, wherein said first and said second layer thicknesses are dimensioned such that $d_1 \leq 0.3d_2$.

5. The process according to claim 2, wherein applying the layer of conductive material over the insulator layer includes depositing the layer of conductive material over the insulator layer, and partially removing the layer of conductive material from over said field regions to establish a desired thickness differential between the first and second layer thicknesses.

6. The process according to claim 2, wherein applying the layer of conductive material over the insulator layer includes depositing a planarized layer of conductive material over the insulator layer to establish a desired thickness differential between the first and second layer thicknesses.

7. The process according to claim 5, wherein said first layer thickness and said second layer thickness are dimensioned such that $d_1 \leq 0.5d_2$, with d_1 being said first layer thickness and d_2 being said second layer thickness.

8. The process according to claim 7, wherein said first and said second layer thicknesses are dimensioned such that $d_1 \leq 0.3d_2$.

9. The process according to claim 6, wherein said first layer thickness and said second layer thickness are dimensioned such that $d_1 \leq 0.5d_2$, with d_1 being said first layer thickness and d_2 being said second layer thickness.

10. The process according to claim 9, wherein said first and said second layer thicknesses are dimensioned such that $d_1 \leq 0.3d_2$.

11. The process according to claim 1, wherein said conductive material is copper.

12. The process according to claim 1, wherein said conductive material is a copper alloy.

13. The process according to claim 1, wherein removing the excess conductive material is done by chemical mechanical polishing, chemical etching, electrochemical etching, or any combination of chemical mechanical polishing, chemical etching and electrochemical etching.

14. The process according to claim 1, wherein establishing said grain size differential also establishes a differential in chemical removal rates, physical removal rates, or both chemical and physical removal rates at which the excess conductive material

can be removed from over said field regions and over said features.